PCF8802

Smartcard RTC; ultra low power oscillator with integrated counter for initiating one time password generation

Rev. 1 — 30 June 2014 Product data sheet

1. General description

The PCF8802 is a CMOS integrated circuit for battery operation, typically supplied by button cells or flexible polymer batteries. Incorporated is a 32.768 kHz quartz crystal oscillator circuit including the two load capacitors. The circuit is optimized for a quartz with 6 pF load capacitance specification. Higher values can also be used with the addition of external load capacitors.

The main function of the oscillator is to generate a $\frac{1}{32}$ Hz clock signal which is used to increment a 24 bit binary counter. The counter can be read over the serial interface and can also be set to any desired value. Control over the divider chain also allows for accurate starting of the counter. Incrementing of the counter value during read is prevented by freezing of the counter during access.

An interrupt signal is also available and is triggered coincident with the counter updating. This signal can be used as a wake-up for a microcontroller.

2. Features and benefits

- 32.768 kHz quartz oscillator, amplitude regulated with excellent frequency stability and high immunity to leakage currents
- Two integrated quartz crystal oscillator capacitors
- Very low current consumption: typically 130 nA
- Two-wire serial interface (I^2C-bus)
- Integrated 24-bit counter with auto increment every 32 seconds
- Interrupt output for processor wake-up
- Stop function for accurate time setting and current saving during shelf life
- User test modes for accelerated application testing and development

3. Applications

- One time password function generators
- Ultra low-power time keeper circuit

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF8802AUG	WLCSP8	wafer level chip-size package; 8 bumps	PCF8802AUG

4.1 Ordering options

Table 2. Ordering options

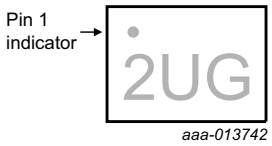
Product type number	Orderable part number	Sales item (12NC)	Delivery form	IC revision
PCF8802AUG/AB[1]	PCF8802AUG/ABZ	935304226027	gold bumps; chips in tape and reel	1

[1] Bump hardness see Table 16.

5. Marking

Table 3. Marking codes

Product type number	Marking code
PCF8802AUG/AB	PC8802-1
	backside (non-active side) laser marking



6. Block diagram

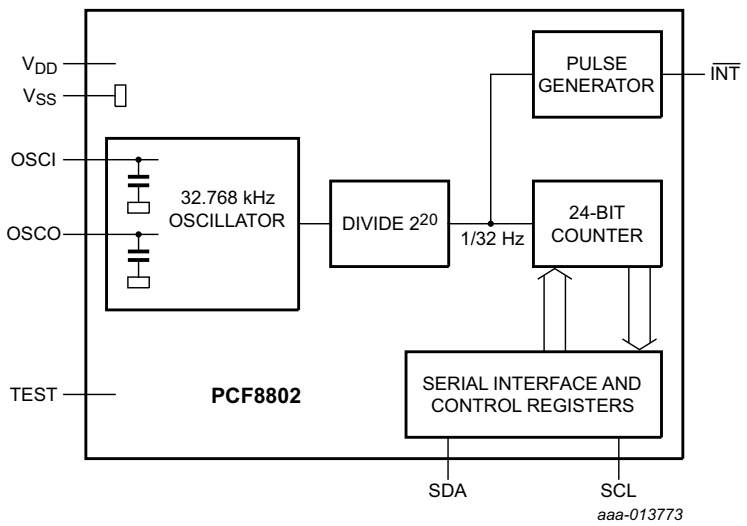
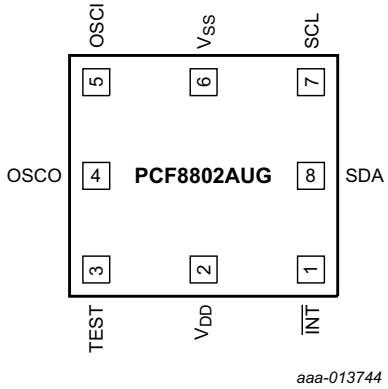


Fig 1. Block diagram of PCF8802

7. Pinning information

7.1 Pinning



Viewed from active side. For mechanical details, see Figure 26.

Fig 2. Pinning diagram of PCF8802AUG

7.2 Pin description

Table 4. Pin description for PCF8802

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin	Description
$\overline{INT}$	1	interrupt and test mode output, push-pull
V_{DD}	2	supply voltage
TEST	3	test pin; must be connected to V_{SS}
OSCO	4	oscillator output
OSCI	5	oscillator input
V_{SS}	6	ground
SCL	7	serial interface, clock
SDA	8	serial interface, bidirectional data line; push-pull

8. Functional description

The PCF8802 is an ultra low-power device for battery operations. The integrated oscillator circuit generates a $^{1}/_{32}$ Hz clock signal to increment a 24-bit counter. The communication between the PCF8802 and other devices is made via point to point I^2C-bus protocol.

The device is always running but for longer storage time it can be put in deep sleep and enabled again in case of delivery.

The functions of the device can be controlled with the following instruction set:

Table 5. Instruction set overview

Instruction	Description	Reference
wrt_cmd	device write access	Section 8.6.2
dvs_cmd	divider start or stop switch	Section 8.6.3
pwd_cmd	deep sleep mode switch	Section 8.6.4
32k_cmd	32.768 kHz clock signal on the pin $\overline{INT}$ switch	Section 8.6.5
fst_cmd	fast system development mode switch	Section 8.6.6
set_cmd	set counter instruction	Section 8.6.7
rd_cmd	counter read instruction	Section 8.6.8

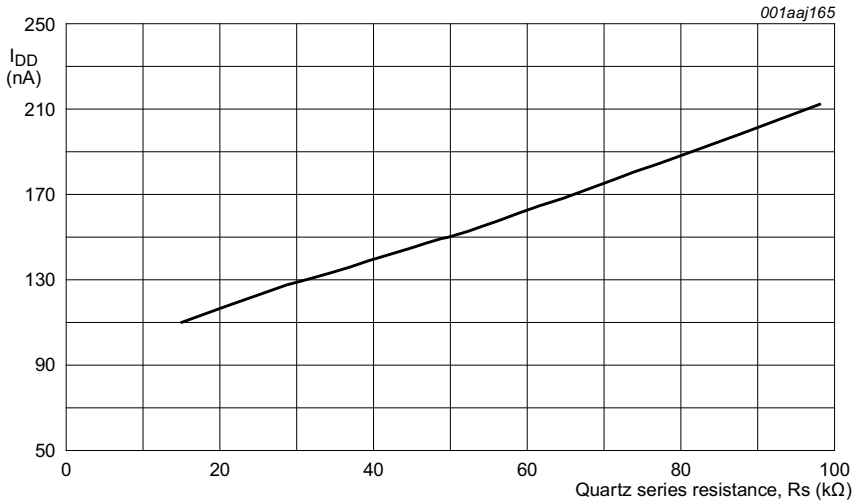
8.1 Oscillator

The 32.768 kHz oscillator includes two integrated load capacitors and an automatic gain control to ensure a reliable start-up.

For prototype development and system debugging, it is possible to output a 32.768 kHz square wave on the $\overline{INT}$ pin with the 32k_cmd instruction.

8.1.1 Low-power operation

When the oscillator is running, a prime consideration for low power consumption is the series resistance R_S of the quartz used. The series resistance acts as a loss element. Low R_S reduces current consumption further.



V_{DD} = 3 V.

Fig 3. I_{DD} with respect to R_S

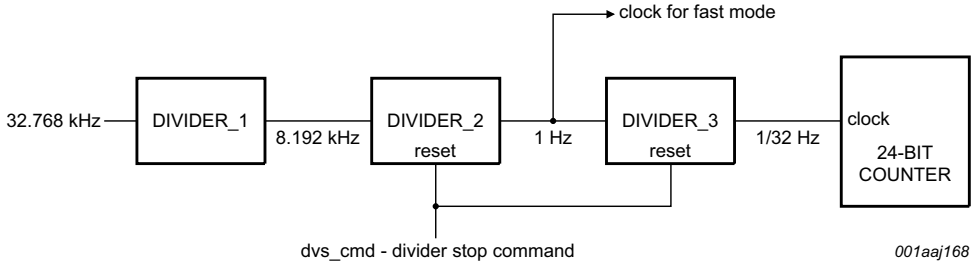
8.1.2 Deep sleep mode

With the deep sleep mode instruction (pwd_cmd) the oscillator can be stopped and the device can be put into a deep sleep where power consumption is reduced to an absolute minimum. An example sequence can be found in Table 8. In deep sleep mode, the interface is still accessible.

8.2 Divider

The divider chain is responsible for reducing the 32.768 kHz oscillator frequency down to $^1/_{32}$ Hz.

The dividers (see Figure 4) divider_2 and divider_3 can be reset with the dvs_cmd instruction. The 24-bit counter can be set when the dividers are held in reset, but this is not a requirement. This allows for accurate setting and restarting of the counter.



Divider_1 = dividing by 4.

Divider_2 = dividing by 8192.

Divider_3 = dividing by 32.

Fig 4. Divider chain

The interface is asynchronous to the quartz oscillator and the state of divider_1 cannot be known when the dvs_cmd is enabled. The 8.192 kHz clock could have just occurred and hence a delay of $^{1}/_{8192}$ seconds will occur before the next increment of the divider_2, or the 8.192 kHz clock could be just about to occur and immediately increment the divider_2.

As a consequence, an uncertainty of between zero and one 8192 Hz clock period (that is, a time uncertainty of about 0 s to 122 μs) will be present when restarting the counter.

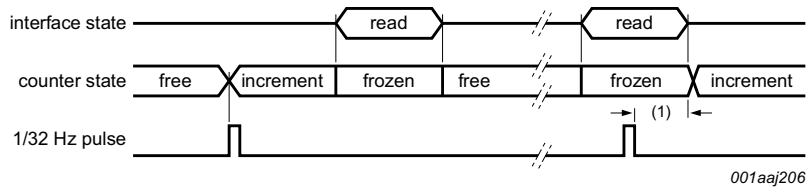
8.3 Binary counter

A 24-bit binary roll-over counter is implemented. The counter is reset at power-on.

The counter can be set to any value using the set_cmd instruction. The set_cmd instruction allows partial writing of data. Partial writing of the data parameters results in partial setting of the counter. For example, if data transfer is stopped after P1[23:16] (see Table 6) is transmitted, then only bit 23 to bit 16 will be updated. The counter will not increment while being set.

The counter can be halted by stopping the dividers using the dvs_cmd instruction.

The counter can be read at any time and the counter value remains stable during reading. If the counter is due to increment during the read or write cycle, then the request to increment will be held off until after the read has concluded. For this reason, it is important to read the counter in bursts, ensuring that an interface STOP condition (see Section 8.5.4) is present between read accesses. Reading for periods of more than 32 seconds at a time results in loss of counts.



(1) Increment delayed until after the read has finished.

Fig 5. Counter behavior during read access

8.4 Pulse generator

An interrupt pulse is available at the $\overline{\text{INT}}$ pin. This pulse is generated once every 32 seconds. It could be used to wake up a microcontroller to perform a periodic function, for example, to calculate and update an LCD display with a new one-time password. A pulse is generated coincident with the increment of the counter. The new counter value is immediately available.

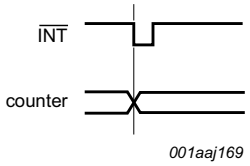


Fig 6. Pulse generator

8.5 I²C-bus interface

For a more detailed information about the I²C-interface, see Ref. 10 “UM10204”

8.5.1 Interface protocol

The serial interface is a point-to-point I²C-bus protocol. The I²C-bus protocol has the advantage of being robust in terms of immunity to electrical noise. Although the PCF8802 does not have the signal filters inside the interface pins, the slave address and acknowledge hand shaking is nevertheless implemented.

For power saving, the SDA output is a push-pull instead of the more traditional open-drain output. Push-pull prevents the need for power consuming pull-up resistors, but requires that the SDA line of the microcontroller is a push-pull as well[1] and does limit the operation to point-to-point only.

The following slave addresses plus a write and read bit are reserved for the PCF8802:

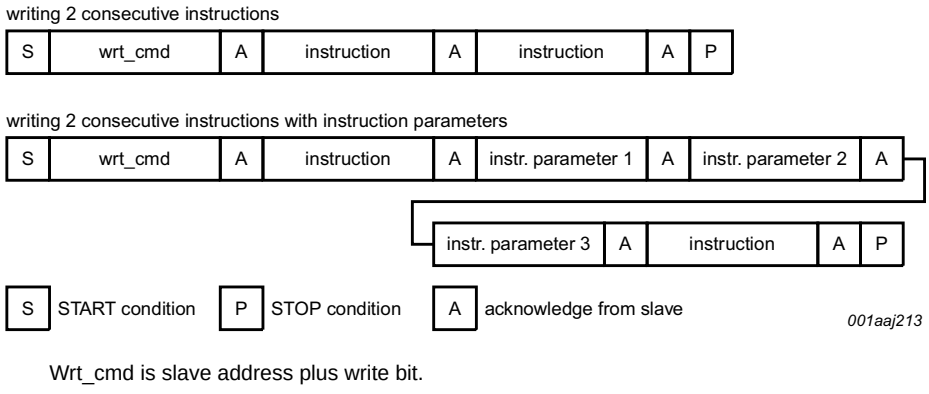
- write: 1010 0000
- read: 1010 0001

An incorrect slave address results in the device ignoring all bus data. A STOP or START condition (see Section 8.5.4) is required before a new transfer can be made.

8.5.1.1 The writing protocol

The writing protocol is shown in Figure 7.

There is no restriction for the order of sending instructions. As many instructions as needed can be sent in one access. The total duration of one access must not exceed 32 seconds (see Figure 9).



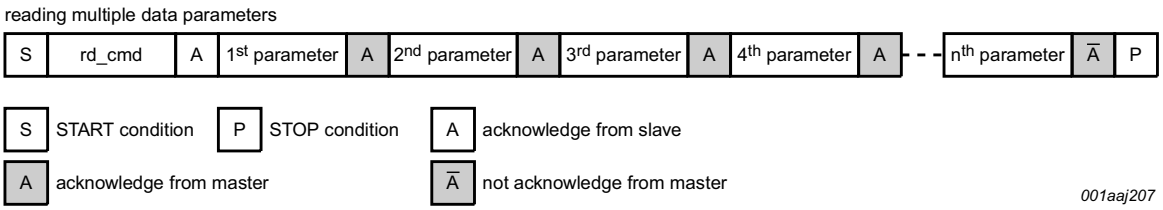
Wrt_cmd is slave address plus write bit.

Fig 7. Writing protocol

1. If the SDA line on the microcontroller is open drain a pull-up resistor is needed.

8.5.1.2 The reading protocol

The reading protocol is shown in Figure 8.

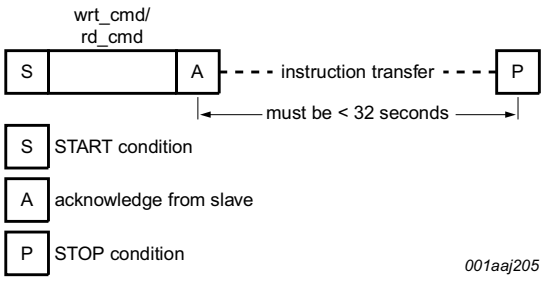


Rd_cmd is slave address plus read bit.

Fig 8. Reading protocol

8.5.1.3 Reading and writing limitations

As the counter is frozen during interface accesses, all accesses must be completed within 32 seconds (see Figure 9). If this rule is not adhered to, then counts are dropped.



Wrt_cmd is slave address plus write bit.

Rd_cmd is slave address plus read bit.

Fig 9. Access restrictions

8.5.2 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time are interpreted as a control signal. Bit transfer is shown in Figure 10.

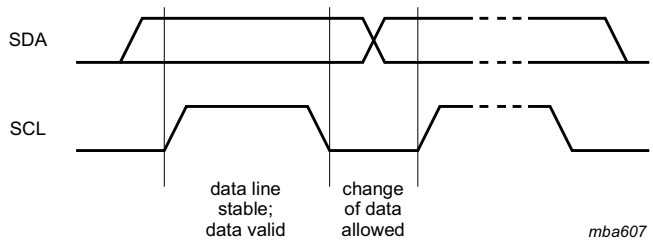


Fig 10. Bit transfer

8.5.3 Bit order

Data is transferred MSB first.

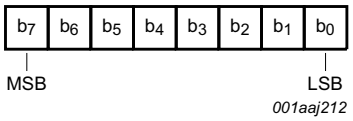


Fig 11. Bit transfer

8.5.4 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are shown in Figure 12.

The data on SDA is sampled with the rising edge of SCL. Data is output to SDA on the falling edge of SCL.

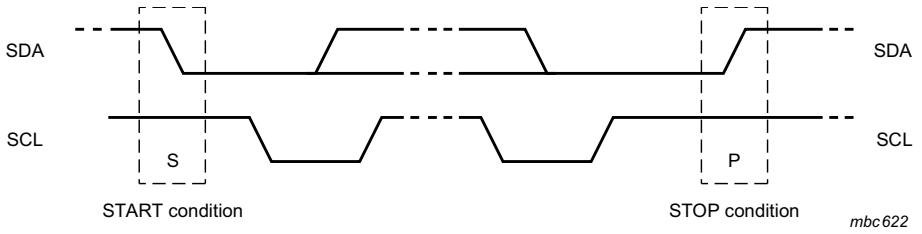


Fig 12. Definition of START and STOP conditions

8.5.5 System configuration

A device generating a message is a transmitter, a device receiving a message is the receiver. The device that controls the message is the master and the device which is controlled by the master is the slave.

8.5.6 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. But the duration of the access must not exceed 32 seconds. Each byte of 8 bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be considered). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement is shown in Figure 13.

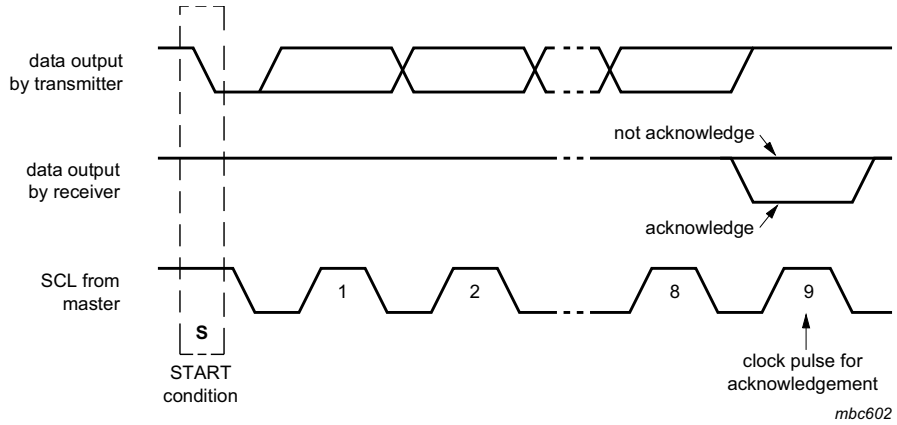


Fig 13. Acknowledgement on the I²C-bus

8.5.7 Data transfer

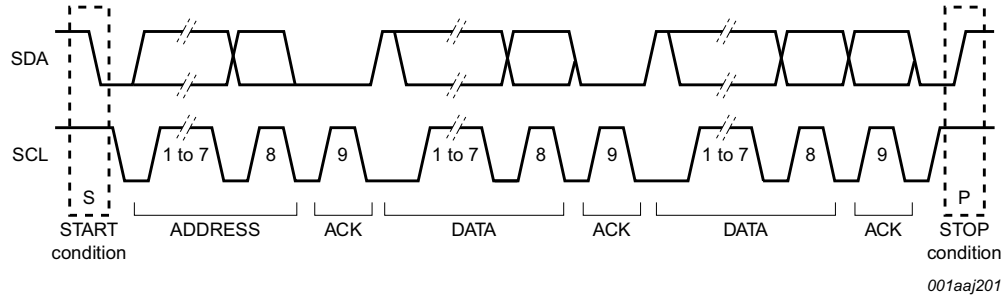


Fig 14. A complete data transfer

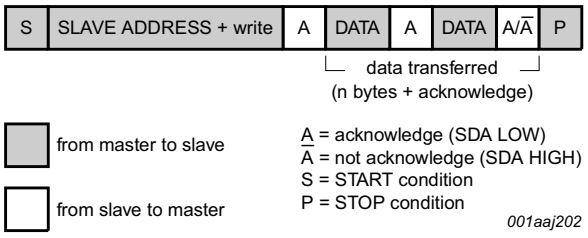


Fig 15. A master-transmitter addresses a slave receiver

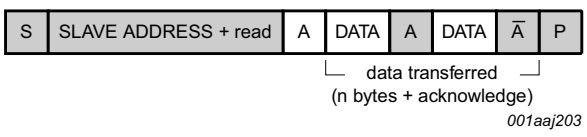
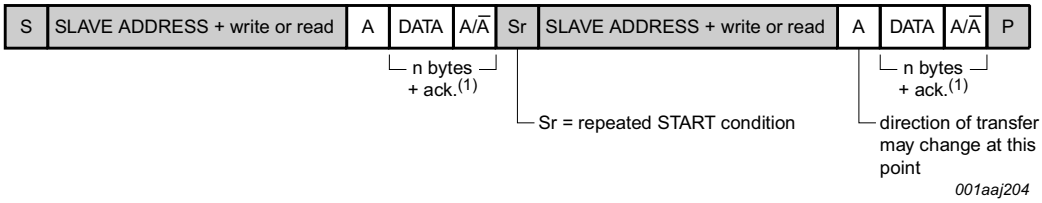


Fig 16. A master reads from a slave immediately after the first byte

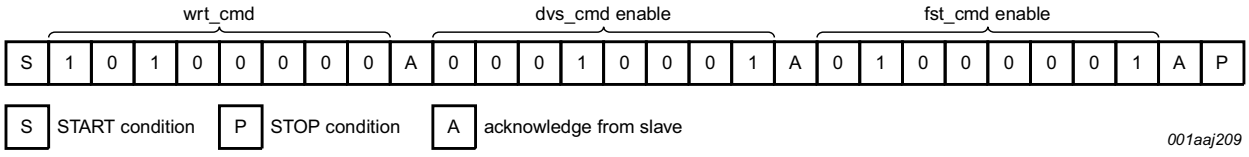


(1) Not shaded because transfer direction of data and acknowledge bits depends on R/$\overline{W}$ bits.

Fig 17. Combined format

8.5.7.1 Example data transfers

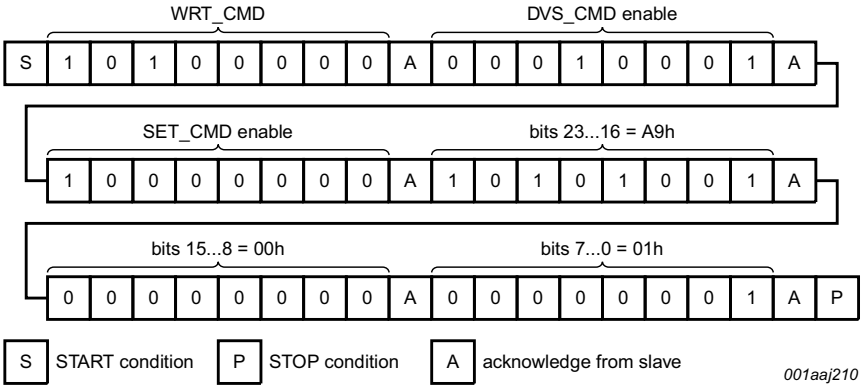
Example 1: Sending the instruction dvs_cmd followed by fst_cmd is shown in Figure 18.



Wrt_cmd is slave address plus write bit.

Fig 18. Sending instructions

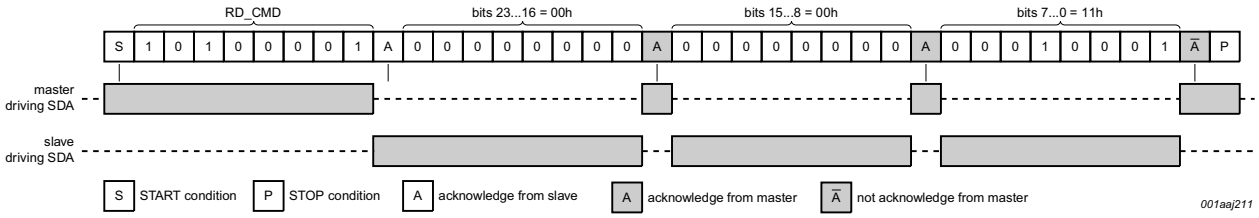
Example 2: Sending dvs_cmd followed by setting the counter to A90001h is shown in Figure 19



Wrt_cmd is slave address plus write bit.

Fig 19. Setting the counter

Example 3: Reading the counter (counter = 000011h) is shown in Figure 20.



Rd_cmd is slave address plus read bit.

Fig 20. Reading the counter

8.6 Instructions

8.6.1 Instruction set

Table 6. Write instructions

The writing protocol is illustrated in Figure 7.

First byte		Second byte		Further bytes	Action
Instruction	**Instruction code**	**Instruction**	**Instruction code**	**Parameters**	
wrt_cmd	1010 0000			-	device slave write address: slave address plus write bit
		dvs_cmd	0001 0001	-	stop and reset dividers
			0001 0000	-	start dividers
		pwd_cmd	0010 0001	-	shut down the device
			0010 0000	-	enable the device
		32k_cmd	0011 0001	-	enable output of 32.768 kHz on pin $\overline{\text{INT}}$
			0011 0000	-	disable output of 32.768 kHz on pin $\overline{\text{INT}}$
		fst_cmd	0100 0001	-	fast mode; increments counter every second
			0100 0000	-	fast mode disable
		set_cmd	1000 0000		set the counter value
				P1[23:16]	parameter with counter values
				P2[15:8]	
				P3[7:0]	

Table 7. Read instructions

The reading protocol is illustrated in Figure 8.

First byte		Further bytes	Action
Instruction	**Instruction code**	**Parameters**	
rd_cmd[1]	1010 0001		device slave read address: slave address plus read bit
		P1[23:16]	parameter with counter values; continues to read until no ACK is received; counter is not updated during this time
		P2[15:8]	
		P3[7:0]	
		P4[23:16]	
		:	

[1] Read of the counter is implicit with an interface read.

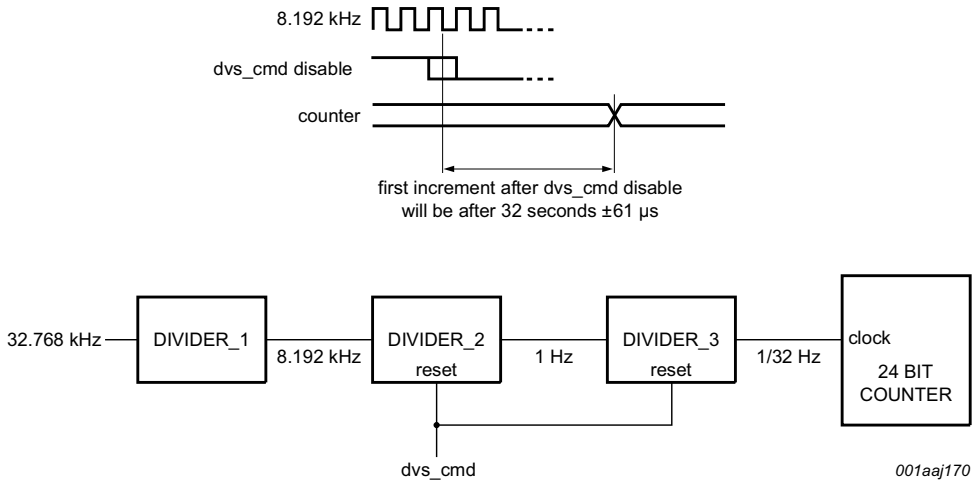
8.6.2 Instruction wrt_cmd

The write instruction (wrt_cmd) precedes each write sequence. Details of the writing protocol can be found in Section 8.5.1.1.

8.6.3 Instruction dvs_cmd

The divider stop instruction (dvs_cmd) can be used to freeze the divider chain and to put it in a defined state. The first 2 bits of the divider chain cannot be influenced. With this instruction, it is possible to control the time to the next increment of the counter. See Table 9.

When the dividers are restarted, the first increment of the 24-bit counter will be after 32 seconds.



Divider_1 = dividing by 4.

Divider_2 = dividing by 8192.

Divider_3 = dividing by 32.

Fig 21. Instruction dvs_cmd

When the dividers are restarted, the 8192 Hz clock could have just occurred and hence a delay of $1/8192$ seconds will occur before the next increment of the divider_2. Or the 8192 Hz clock could be just about to occur and immediately increment the divider_2. As a consequence, an uncertainty of one half clock period in the starting of the 24 bit counter is present when restarting (see Figure 21).

8.6.4 Instruction pwd_cmd

The power down instruction (pwd_cmd) is intended to be used to put the system into a low-power mode for storage. Static leakage current will be the only power consumed. Storage at temperatures exceeding room temperature can increase leakage currents.

Entering deep sleep mode requires a specific sequence of events since under normal circumstances stopping the oscillator would result in a chip reset.

Table 8. Deep sleep mode sequence

Step	Action	Code sequence	Note
To enter deep sleep mode			
1	initiate transfer	START condition	-
2	send wrt_cmd	1010 0000	-
3	enable dvs_cmd	0001 0001	stop the divider
4	set counter with set_cmd	1000 0000	set the counter = AAAAAAh
		1010 1010	P1[23:16]
		1010 1010	P2[15:8]
		1010 1010	P3[7:0]
5	enable pwd_cmd	0010 0001	stop the oscillator
6	end transfer	STOP condition	-
7	device is now in deep sleep mode	-	-
To exit deep sleep mode			
1	initiate transfer	START condition	-
2	send wrt_cmd	1010 0000	-
3	disable pwd_cmd	0010 0000	oscillator starts on the ACK cycle of this instruction
4	disable dvs_cmd	0001 0000	enable the divider again
5	end transfer	STOP condition	-

8.6.5 Instruction 32k_cmd

The 32.768 kHz enable instruction (32k_cmd) is intended to aid with oscillator characterization during system development. With this instruction, it is possible to obtain a 32.768 kHz clock on the $\overline{INT}$ pin which can be used for measurement.

This mode does not affect other operation of the chip except for the loss of interrupt output.

8.6.6 Instruction fst_cmd

The fast mode instruction (fst_cmd) is intended to enable faster system development. When enabled, the counter increments once every second instead of once every 32 seconds. Interrupt pulses are generated once every second as well.

When using fst_cmd, data access to the device must be completed within 1 second, if not then counter increments are lost. The 1 second period is measured from the ACK cycle of a valid slave address to the next STOP or repeated START. A repeated START is sufficient to allow the counter to increment.

8.6.7 Instruction set_cmd

The counter can be set to any value using the set instruction (set_cmd). Partial writing of the data parameters results in partial setting of the counter. For example, if data transfer is stopped after P1[23:16] is transmitted, then only bit 23 to bit 16 will be updated.

This instruction takes only 3 parameters in one command. Data after the third parameter are interpreted as the next instruction.

Accurate setting and start-up can be implemented using the dvs_cmd instruction in cooperation with the set_cmd instruction. An example is shown in Table 9.

Table 9. Example of accurate setting of the counter

Step	Action	Code sequence	Note
1	initiate transfer	START condition	-
2	send wrt_cmd	1010 0000	-
3	enable dvs_cmd	0001 0001	-
4	set counter with set_cmd	1000 0000	set the counter = 1
		0000 0000	P1[23:16]
		0000 0000	P2[15:8]
		0000 0001	P3[7:0]
5	end transfer	STOP condition	-
6	wait for an external time marker	-	-
7	initiate transfer	START condition	-
8	send wrt_cmd	1010 0000	-
9	disable dvs_cmd	0001 0000	counter starts on the ACK cycle of this instruction
10	end transfer	STOP condition	-

8.6.8 Instruction rd_cmd

With the read instruction (rd_cmd) the counter value can be read at any time. When the counter value is read, the counter is frozen so that there are no changes during the read back. After a read is terminated, the counter will be allowed to increment again. Any increment that was scheduled during the frozen period will then be effected.

Reading the counter is cyclic, that is, the device repeatedly returns the present counter value until the read is terminated. Reading the counter more than once can be useful in the case that the application is subject to a strong Electromagnetic Interference (EMI) environment, so that read-back values can be compared.

Read back must be terminated within 32 seconds else a count will be dropped.

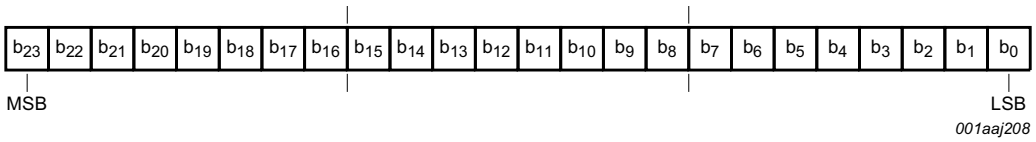


Fig 22. Read bit order

8.7 Power-on reset

At initial power-on a reset is generated. The reset lasts not longer than 10 ms. During this time, the serial interface will not respond when accessed. The state of the device after power-on reset is shown in Table 10.

Table 10. Reset state

Instruction name	State after reset
dvs_cmd	disabled
pwd_cmd	disabled
32k_cmd	disabled
fst_cmd	disabled
24-bit counter	000000h

9. Internal circuitry

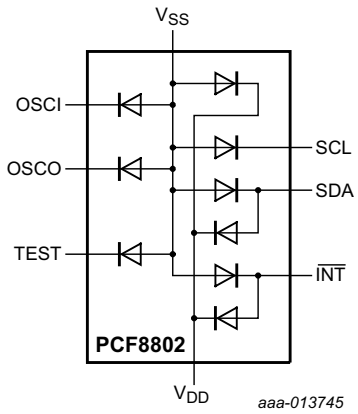


Fig 23. Diode protection diagram

10. Safety notes

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

CAUTION

Semiconductors are light sensitive. Exposure to light sources can cause the IC to malfunction. The IC must be protected against light. The protection must be applied to all sides of the IC.

11. Limiting values

Table 11. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+6.5	V
I_{DD}	supply current		–50	+50	mA
V_I	input voltage		–0.5	+6.5	V
I_I	input current		–10	+10	mA
V_O	output voltage		–0.5	+6.5	V
I_O	output current		–10	+10	mA
P_{tot}	total power dissipation		-	300	mW
V_{esd}	electrostatic discharge voltage	HBM [1]	-	±2500	V
		MM [2]	-	±200	V
I_{lu}	latch-up current	[3]	-	200	mA
T_{amb}	ambient temperature		–40	+85	°C
T_{stg}	storage temperature	[4]	–65	+150	°C

[1] Pass level; Human Body Model (HBM) according to JESD22-A114.

[2] Pass level; Machine Model (MM), according to JESD22-A115.

[3] Pass level; Latch-up testing, according to JESD78.

[4] According to the store and transport requirements (see Ref. 11 “UM10569”) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

12. Static characteristics

Table 12. Static characteristics

V_{DD} = 1.6 V to 5.5 V; V_{SS} = 0 V; f_{osc} = 32.768 kHz; T_{amb} = −40 °C to +85 °C; quartz crystal: R_s = 30 kΩ, C_L = 6.0 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DD}	supply voltage		1.6	-	5.5	V
		T_{amb} = 25 °C; f_{SCL} = 0 Hz	-	1.0	-	V
ΔV_{DD}	supply voltage variation	$\Delta V/\Delta t$ = 1 V/µs	-	0.25	-	V
I_{DD}	supply current	deep sleep active [1]				
		T_{amb} = 25 °C; V_{DD} = 3 V; f_{SCL} = 0 Hz	-	3	-	nA
		device running				
		f_{SCL} = 0 Hz	-	-	400	nA
		T_{amb} = 25 °C; V_{DD} = 3 V; f_{SCL} = 0 Hz	-	130	-	nA
		interface active				
		f_{SCL} = 100 kHz	-	5	20	µA
		f_{SCL} = 1 MHz	-	50	100	µA
Oscillator						
V_{start}	start voltage		-	1.1	-	V
$t_{startup}$	start-up time		-	0.2	-	s
$C_{L(itg)}$	integrated load capacitance	[2]	-	6.0	-	pF
Inputs						
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	-	V
V_I	input voltage	on pins SCL, OSCI, TEST	−0.5	-	5.5	V
		on pin SDA	−0.5	-	V_{DD} + 0.5	V
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}; on pins SCL, SDA and TEST	−200	0	+200	nA
Outputs						
V_O	output voltage		−0.5	-	V_{DD}+0.5	V
I_{OH}	HIGH-level output current	V_{OH} = 4.0 V; V_{DD} = 5 V; on pins $\overline{INT}$ and SDA	-	5	2	mA
		V_{OH} = 1.28 V; V_{DD} = 1.6 V; on pins $\overline{INT}$ and SDA	-	0.5	0.2	mA

Table 12. Static characteristics *...continued*

V_{DD} = 1.6 V to 5.5 V; V_{SS} = 0 V; f_{osc} = 32.768 kHz; T_{amb} = −40 °C to +85 °C; quartz crystal: R_s = 30 kΩ, C_L = 6.0 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{OL}	LOW-level output current	V_{OL} = 1.0 V; V_{DD} = 5 V; on pins $\overline{INT}$ and SDA	−2	−7	-	mA
		V_{OL} = 0.32 V; V_{DD} = 1.6 V; on pins $\overline{INT}$ and SDA	−0.4	−1	-	mA
I_{LO}	output leakage current	V_O = V_{DD} or V_{SS}; on pins SDA and $\overline{INT}$	−200	0	+200	nA

[1] Unless otherwise defined, I_{DD} is measured with the reset state, see Section 8.7.

[2] Integrated load capacitance, $C_{L(itg)}$, is a calculation of C_{OSCI} and C_{OSCO} in series: $C_{L(itg)} = \frac{(C_{OSCI} \cdot C_{OSCO})}{(C_{OSCI} + C_{OSCO})}$.

13. Dynamic characteristics

Table 13. Dynamic characteristics

V_{DD} = 1.6 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified. [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Timing characteristics: serial bus						
f_{SCL}	SCL clock frequency		-	-	1	MHz
t_{LOW}	LOW period of the SCL clock		500	-	-	ns
t_{HIGH}	HIGH period of the SCL clock		260	-	-	ns
t_{BUF}	bus free time between a STOP and START condition		500	-	-	ns
$t_{HD;STA}$	hold time (repeated) START condition		260	-	-	ns
$t_{SU;STA}$	set-up time for a repeated START condition		260	-	-	ns
t_r	rise time of both SDA and SCL signals	[2]	-	10	-	ns
t_f	fall time of both SDA and SCL signals	[2]	-	10	-	ns
$t_{SU;DAT}$	data set-up time		50	-	-	ns
$t_{HD;DAT}$	data hold time		0	-	-	ns
$t_{SU;STO}$	set-up time for STOP condition		260	-	-	ns
$t_{VD;DAT}$	data valid time		75	-	450	ns
C_b	capacitive load for each bus line		-	-	50	pF
Timing characteristics: $\overline{INT}$						
$t_{w(int)}$	interrupt pulse width		20	40	80	µs

[1] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

[2] Rise and fall times are not limited. Fast edges can lead to system EMI problems, while slow edges are susceptible to noise.

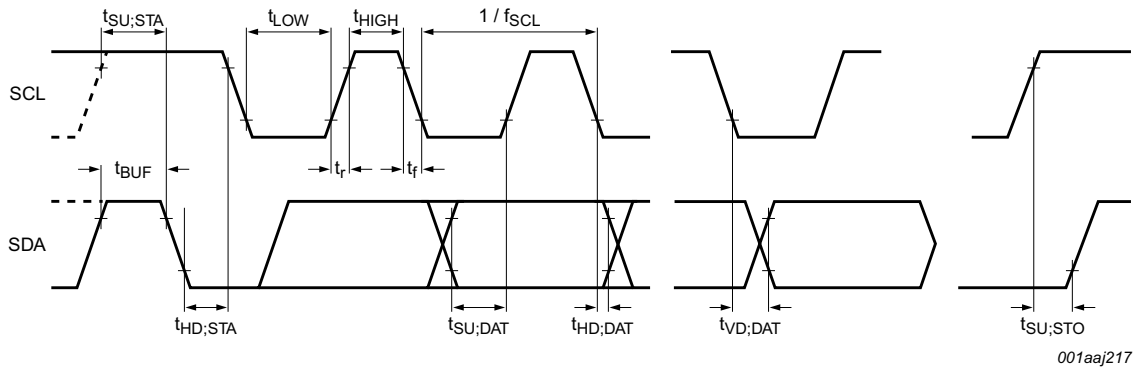


Fig 24. Serial bus timing waveforms

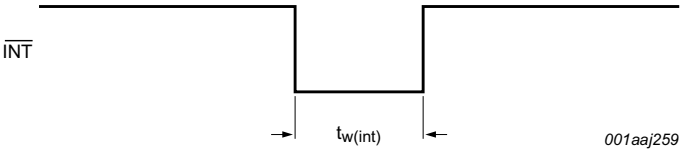
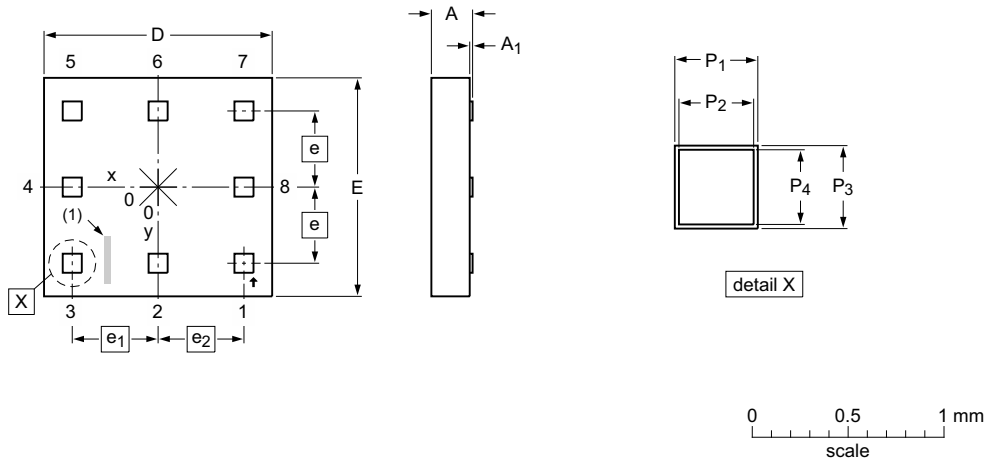


Fig 25. $\overline{\text{INT}}$ timing

14. Bare die outline

WLCSP8: wafer level chip-size package; 8 bumps **PCF8802AUG**



Notes
1. Marking code: PC8802-1.

pcf8802aug_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCF8802AUG						~~14-06-18~~ 14-06-20

Fig 26. Bare die outline PCF8802AUG

Table 14. Dimensions of PCF8802AUG

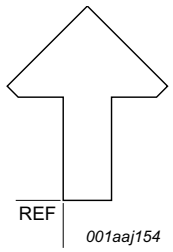
Original dimensions are in mm.

Unit (mm)	A	A_1	D[1]	E[1]	e	e_1	e_2	P_1[2]	P_2[3]	P_3[2]	P_4[3]
max	-	0.018	-	-	-	-	-	-	0.093	-	0.093
nom	0.215	0.015	1.19	1.14	0.396	0.448	0.449	0.099	0.090	0.099	0.090
min	-	0.012	-	-	-	-	-	-	0.087	-	0.087

[1] Including saw lane.

[2] Pad size.

[3] Bump size.



Pin 1 is identified by this symbol.

Fig 27. Pin 1 identifier

Table 15. Bump and reference point locations of PCF8802AUG

Symbol	Pad	Coordinates[1]	
		x	y
$\overline{INT}$	1	437	−396
V_{DD}	2	−12	−430
TEST	3	−460	−396
OSCO	4	−460	1
OSCI	5	−460	396
V_{SS}[2]	6	−12	430
SCL	7	437	396
SDA	8	437	1
pin 1 identifier	-	474.7	−472.0
bottom left die corner[3]	-	−594.8	−568.2
top right die corner[3]	-	594.7	568.3

[1] All coordinates are referenced, in μm, to the center of the die (see Figure 26).

[2] The substrate (rear side of the die) is connected to V_{SS} and should be electrically isolated.

[3] Die size before dicing. Final dimensions will be 10 μm to 20 μm smaller.

Table 16. Gold bump hardness of PCF8802AUG

Gold bump type	Min	Max	Unit[1]
soft gold bump	35	80	HV

[1] Pressure of diamond head: 10 g to 50 g.

15. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

16. Packing information

16.1 Tape and reel information for PCF8802AUG

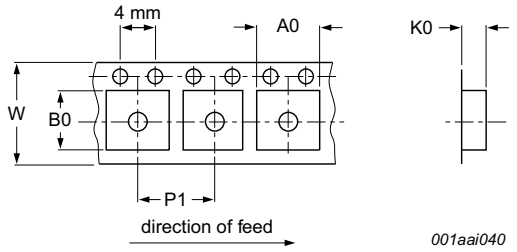
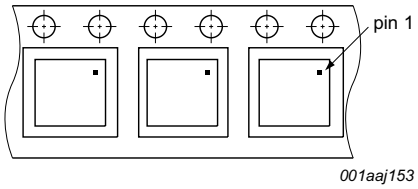


Fig 28. Tape and reel details for PCF8802AUG

Table 17. Tape and reel dimensions

Dimension	Description	Value	Unit
W	tape width	8.0 (–0.1, +0.3)	mm
A0	pocked length	1.29 (± 0.05)	mm
B0	pocket width	1.34 (± 0.05)	mm
K0	pocket depth	0.37 (± 0.05)	mm
P1	pocket pitch	4.0 (± 0.1)	mm



Die is placed in pocket bump side down.

The orientation of the IC in a pocket is indicated by the position of pin 1, with respect to the sprocket holes (see Table 3 on page 2 for pin 1 indicator on the backside marking).

Fig 29. Pocket alignment for PCF8802AUG

17. Abbreviations

Table 18. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
EMI	ElectroMagnetic Interference
HBM	Human Body Model
IC	Integrated Circuit
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit
PCB	Printed-Circuit Board
RTC	Real-Time Clock
WLCSP	Wafer Level Chip-Size Package

18. References

[1] **AN10439 —** Wafer Level Chip Size Package

[2] **AN10706 —** Handling bare die

[3] **AN10853 —** ESD and EMC sensitivity of IC

[4] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[5] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[6] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[7] **JESD22-A115 —** Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)

[8] **JESD78 —** IC Latch-Up Test

[9] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[10] **UM10204 —** I^2C-bus specification and user manual

[11] **UM10569 —** Store and transport requirements

19. Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF8802 v.1	20140630	Product data sheet	-	-

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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